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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,460	06/12/2006	Uli Joos	TM010	2099

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CONTINENTAL TEVES, INC.
ONE CONTINENTAL DRIVE
AUBURN HILLLS, MI 48326-1581

EXAMINER	
DEBERADINIS, ROBERT L	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,460	JOOS ET AL.	
	Examiner	Art Unit	
	Robert DeBeradinis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-18,20-22 and 24* is/are rejected.

7)☒ Claim(s) *19 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-18,20-22,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over NAKAMURA et al. 6,891,342.

CLAIM 13

NAKAMURA et al. discloses a method for pulse width modulated control of a plurality of load elements, the load elements being controlled in time staggered manner with respect to each other, the method comprising:

controlling the load elements by a common control unit (34) with a common system clock (not shown but obviously being the ECU 32 is a microcomputer based system one of ordinary skill in the art would realize that the clock would obviously be the reference of timing) in phase staggered manner (fig. 8B);

predetermining, for each load element, an initial value and a final value, wherein the initial values of the load elements diverge from each other and the final values of the load elements are determined the switching criteria as disclosed in according to fig. 8B, col. 2, lines 25 plus; and

supplying each load element with current for a period of time between the respective initial and final value.

NAKAMURA et al. does not disclose the pulse-break ratio.

It would have been obvious to one having ordinary skill in the art at the time of the invention to have derived the pulse break ratio with the knowledge

of the teaching as disclosed in fig. 8B, col. 2, lines 25 plus in the event that more than two loads where to be driven resulting in generating the least amount of electrical ripple.

CLAIMS 14,18

NAKAMURA et al. discloses the method according to claim 13, wherein the load elements are inductive in an electrically independent load circuit and are supplied from a common supply line.

NAKAMURA et al. does not disclose wherein load elements are resistive load elements.

It would have been obvious to one having ordinary skill in the art to have used the drive apparatus to drive resistive loads that are obviously easer to drive than inductive loads and the apparatus and method would work equally as well driving a resistive load.

CLAIMS 15,16

NAKAMURA et al. discloses the method according to claim 13.

NAKAMURA et al. does not disclose wherein a common system clock in a common counter is counted up to a predetermined counter final value.

The Examiner takes official notice, counters are well known in the art and their use to count to a predetermined counter value and to initiate a command is well known in the art

It would have been obvious to one having ordinary skill in the art to provided the desired pulse timing with a counter and setting a predetermined counter value to set the repetitive interval for energizing the loads.

CLAIM 17

NAKAMURA et al. discloses the method according to claim 13, wherein at least one of the following parameters is determined:

a number of load elements to be currently controlled; or

a pulse width of the load elements to be currently controlled; or

an electrical power input or size proportional thereto of the load elements to be currently controlled with respect to each other; or

a harmonic content in a common supply line timed over the control of all load elements (fig. 8B, col. 2, lines 25 plus).

CLAIMS 20,24

NAKAMURA et al. discloses the control circuit for pulse width modulated control of a plurality of load elements, the load elements being controlled in time staggered manner with respect to each other, the circuit comprising:

NAKAMURA et al. does not disclose a common system clock; and

a storage region for each load element, wherein a pulse width and a phase position of the respective load element are stored.

NAKAMURA et al. teaches a microcomputer based system wherein the common system clock would be obviously part of the system.

The Examiner takes official notice, it is well known in the art that a computer based system stores operational data it its storage system to control timing etc. of the sub systems it controls.

It would have been obvious to one having ordinary skill in the art at the time of the invention to have provided the controlled timing from the computer storage system in place of the common counter to save hardware and to reduce cost when the computer storage space is available.

CLAIM 21

NAKAMURA et al. discloses the control circuit according to claim 20 further comprising:

an initial value and final value for the phase staggered pulse width modulated control are stored;

a common counter, which counts the system clock up to a predetermined counter final value;

or each load element storage region an initial value and a final value are stored for the phase staggered pulse width modulated control; and

for each load element a comparator and a switch, which compares the counter state with the initial and final value and dependent therefrom controls the switch in the electric circuit to the load element (same rejection reasoning as claim 20 above).

CLAIM 22

NAKAMURA et al. discloses the control circuit according to claim 21, wherein a reset-input is provided at the counter, by which for all load elements the control can be jointly synchronized by resetting and restarting the counter.

The Examiner takes official notice, it is well known that a reset input is common to a counter and it is also well known that a reset restarts the counter, the synchronizing of the loads is obvious since the counters have a

common clock therefore the load element switching is obviously jointly synchronized, obvious because the counters have the same clock input.

Allowable Subject Matter

Claims 19,23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication should be directed to Robert L. DeBeradinis whose number is (571) 272-2049. The Examiner can normally be reached Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Michael Sherry, can be reached on (571) 272-2084. The Fax phone number for this Group is (571) 272-8300.

RLD

May 10, 2008

/Robert DeBeradinis/

Primary Examiner, Art Unit 2836